AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An apparatus, comprising:

a communication path to exchange information packets;

an integrated circuit die, including:

[a]] an ingress processor to process information packets [[;]] ,

an egress processor to process information packets,

a control plane processor coupled to the ingress and egress processors, and

a buffer pool cache ~~local to the processor~~ coupled to the control plan processor to store free buffer handles for information packets if the buffer pool cache local to the processor is not full; and

a non-local memory to store the free buffer handles for information packets if the buffer pool cache local to the processor is full.

2. (Canceled)

3. (Currently Amended) The apparatus of claim 1, wherein the communication path comprises:

an input coupled to the ingress processor path for receiving information packets; and

an output path coupled to the egress processor for transmitting information packets.

4. (Original) The apparatus of claim 1, wherein the communication path comprises:

a memory path for fetching and freeing buffers.

5-6. (Canceled)

7. (Original) The apparatus of claim 1, wherein the communication path connects to at least one of a dynamic random access memory and a static random access memory.

8. (Original) The apparatus of claim 1, wherein the buffer pool cache is a set of next neighbor registers configured to form a next neighbor ring.

9. (Previously Presented) The apparatus of claim 1, further comprising:

a communication interface device coupled to the communication path.

10. (Currently Amended) A method, comprising:

receiving an information packet via an ingress processor;

fetching, from a local buffer pool cache to the ingress processor via a control plane processor, a buffer handle to be associated with the information packet if the local buffer pool is non-empty; and

fetching the buffer handle from a non-local memory if the local buffer pool cache is empty.

11. (Original) The method of claim 10, further comprising:

storing the information packet in a buffer associated with the fetched buffer handle.

12. (Currently Amended) The method of claim 11, further comprising:

processing the information packet;

transmitting the information packet via an egress processor; and

freeing the buffer handle to the local buffer pool cache.

13. (Canceled)

14. (Original) The method of claim 12, further comprising:

freeing the buffer handle to a non-local memory when the local buffer pool cache is full.

15. (Original) The method of claim 12, wherein the local buffer pool cache is a set of next neighbor registers configured to form a next neighbor ring.

16. (Canceled)

17. (Currently Amended) An apparatus, comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving an information packet at an ingress processor;

fetching, from a local buffer pool cache to the ingress processor via a control plane processor, a buffer handle to be associated with the information packet if the local buffer pool is non-empty; and

fetching the buffer handle from a non-local memory if the local buffer pool cache is empty.

18. (Original) The apparatus of claim 17, wherein execution of the instructions further results in:

storing the information packet in a buffer associated with the fetched buffer handle.

19. (Original) The apparatus of claim 18, wherein execution of the instructions further results in:

processing the information packet;

transmitting the information packet; and

freeing the buffer handle to the local buffer pool cache.

20. (Currently Amended) A system, comprising:

a network processor, including:

a communication path to exchange information packets[[,]] ;

an integrated circuit die, including:

[a]] an ingress processor to process information packets [[;]] ,

an egress processor to process information packets,

a control plane processor coupled to the ingress and egress processors, and

a buffer pool cache ~~local to the processor~~ coupled to the control plan processor to store free buffer handles for information packets if the buffer pool cache local to the processor is not full; and

a non-local memory to store the free buffer handles for information packets if the buffer pool cache local to the processor is full; and

an asynchronous transfer mode interface.

21. (Canceled)